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(54) Packet identifier (PID) aliasing for a broadband audio, video and data router

(57) An efficient, integrated solution for providing packet identifier (PID) aliasing for input transport streams, such as MPEG2 streams. MPEG packets with their original packet identifiers (PIDs) are encapsulated using a customized Internet Protocol (IP)-like scheme, and routed from an input circuit card to one or more various target processor cards in a chassis. The encapsulating packet includes a destination address field that provides source information regarding the received packet, such as a source slot and port, and the original PID. At the processor card, the source information is used by a router to look up a PID alias value, which is then inserted into another field of the encapsulating packet. The encapsulating packet is routed to a PID alias function, which replaces the original PID in the MPEG packet with the alias value. The MPEG packet is then decapsulated, e.g., for further processing on the card. The router may also look up a processing path to route the encapsulated packet on for the PID aliasing, decapsulation, and further processing, which are each provided in multiple available paths on the processor card.

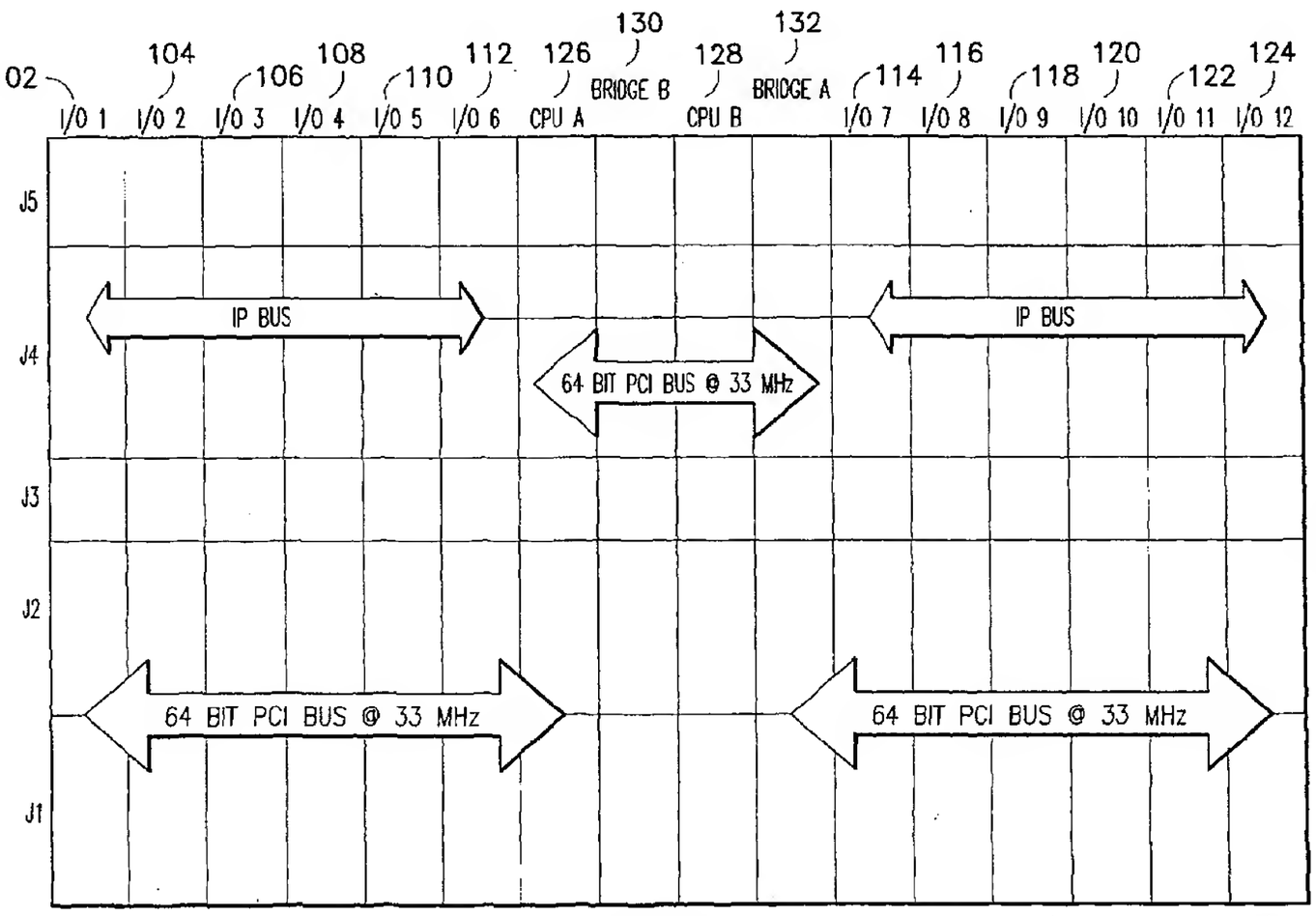

FIG. 1

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to processing of packetized digital data. In particular, PID aliasing is provided for packets of compressed data from input transport streams, such as MPEG data, that are routed to processors on different circuit cards in a chassis (e.g., for transcoding, multiplexing and other processing) using an Internet Protocol (IP)-type routing protocol.

[0002] The following acronyms and terms are used:

ARP -	Address Resolution Protocol
ASI -	Asynchronous Serial Input
ASIC -	Application-Specific Integrated Circuit
BP -	Back Plane
CCA -	Circuit Card Assembly
DPRAM -	Dual Port Random Access Memory
DSP -	Digital Signal Processor
ECM -	Entitlement Control Message
FIFO -	First-In, First Out (buffer)
FPGA -	Field-Programmable Gate Array
HSC -	Hot Swap Controller
IP -	Internet Protocol
MAC -	Medium Access Control
MCG -	Motorola Computer Group
MPEG -	Moving Pictures Expert Group
PCI -	Peripheral Component Interconnect
PHY -	Physical Interface
PID -	Packet Identifier
PMC -	PCI Mezzanine Card
PROM -	Programmable Read-Only Memory
SMII -	Serial Media Independent Interface

[0003] Commonly, it is necessary to process input transport streams, e.g., at a headend of a broadband communication network, such as a cable television network, to provide corresponding output transport streams in a more suitable format. For example, it may be desirable to perform transcoding, splicing (ad insertion or other local programming insertion), multiplexing, encrypting, and PID aliasing. PID aliasing refers to reassigning a PID of an input channel with another value when necessary (e.g., when some channels in the input transport streams have the same PID) to avoid having redundant PIDs in the output transport streams. Or, a PID may be reassigned to correspond with an existing channel map, or for other reasons.

[0004] However, prior systems for processing such input transport streams have not been fully satisfactory. In particular, some systems use discrete hardware that results in a very inflexible architecture. Moreover, components such as multiple DPRAMs are used for PID aliasing, which add significant costs.

[0005] Accordingly, it would be desirable to provide an efficient, integrated solution for processing input transport streams, such as MPEG2 streams.

[0006] PID aliasing should be provided in a system that routes MPEG packets among various CCAs (e.g., boards) in a chassis, which provide functions such as transcoding, multiplexing, splicing, scrambling, and so forth. Customized IP-like routing may be used to route the packets among the cards.

[0007] The system should provide the ability to route any packet to any target MPEG2 processing engine on any board across a backplane of the chassis using multiple routing resources, and the ability to handle PID aliasing in the process.

[0008] The system should provide various benefits, including a quicker time to market, flexibility, and a future proof architecture. The system should preferably use off-the-shelf components that can be readily modified.

[0009] The present invention provides a system having the above and other advantages.

SUMMARY OF THE INVENTION

[0010] The present invention relates to processing of packetized digital data, such as broadband MPEG data.

[0011] The invention involves routing of MPEG packets by encapsulating them over a customized IP packet, and embedding PID alias values within a specified field of the IP packet. Off-the-shelf components may be used. For example, the invention may use a chassis such as MCG's CPX8216IP or CPX1204IP compact PCI chassis. The invention may also use a customized router that is based on a conventional IP router such as the Model LX2212AEC (Intel Corp.), and circuit cards with DSPs which are available from various suppliers. However, the invention is not limited to use with any particular models of components.

[0012] The invention provides a way to move packets of data, such as MPEG2 packets, between different circuit cards in a chassis. Some of the cards are provided with a processor (DSP) for performing any desired processing of the packets. In particular, a customized IP-like routing scheme is used at a router on an input card that receives the packets, e.g., from a remote upstream source, or local source, to encapsulate the packets. The encapsulated packets are routed from the input card to one or more target processor cards.

[0013] The invention may be used with MCG's 8216IP chassis, whose backplane is designed specifically for data traffic on IP from any slot to any slot. MCG's 8216IP 16-slot chassis allows a board-to-board data pathway.

[0014] Moreover, using Intel's LX2212AEC as the IP router enables the ability to embed the PID alias values within the IP packet's destination MAC address. This is achieved by building custom IP header packets. The invention achieves maximum flexibility by providing routing of any PID from multiple MPEG2 transport streams to any target processor chip on any board. Alternatively, the invention can enable an IP router to be used as a router for MPEG data or any other packetized data form.

[0015] The IP router ASIC provides routability of pack-

etized data from any one of, e.g., ten input ports to any MPEG2 processing engine on any board.

[0016] The IP router ASIC along with associated memory is used on every board. The ASIC can be programmed with routing tables and entry tables via PCI. Programming the entry table allows embedding the PID alias value in the destination MAC address field of the IP packet. The next stage is the hardware, which may extract the PID alias value from the customized IP header and replace the MPEG2 packet's PID with it. This reduces memory costs.

[0017] In particular, the invention uses an IP destination address to carry source information of an MPEG packet, such as the slot number, port number and original PID. This is in distinction to the conventional use of a destination address to identify a network card that is to receive a packet. It is possible to carry the source information in other portions of the IP packet.

[0018] An input card router performs a table lookup or the like based on the destination IP address to determine which target board on the chassis the packet is to be routed to. Each output port of the input card's router may be hardwired to a different target board such that an output port identifies the associated target board.

[0019] When the packet is received at the target board (s), it is processed at a processing card router. This router performs a lookup, again based on the destination IP address, to provide a PID alias value in a destination MAC address field of the modified IP packet. The processing card router then passes the packet to the designated target port of a hardware path on the processing card. The modified IP packet is decapsulated, and the PID alias value is substituted for the original PID within the MPEG2 packet. During decapsulation, the IP header is stripped, and the decapsulated MPEG2 packet is sent to a DSP for further processing.

[0020] The routing table within the routers on the different cards contains information that may be configured by a system host computer, e.g., to optimize the use of the processing resources at the cards.

[0021] A target processor card method and apparatus are presented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022]

FIG. 1 illustrates a chassis backplane in accordance with the present invention.
FIG. 2 illustrates a broadband audio/video/data router in accordance with the present invention.
FIG. 3 illustrates the input processor card of FIG. 2 in accordance with the present invention.
FIG. 4(a) illustrates an encapsulated MPEG transport packet in accordance with the present invention.
FIG. 4(b) illustrates a method for routing a packet, and providing PID aliasing, in accordance with the present invention.
FIG. 5 illustrates a processing/DSP card for transcoding, muxing or other processing, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0023] The invention relates to the fields of digital data broadcasting and IP routing.

[0024] FIG. 1 illustrates a chassis backplane 100 in accordance with the present invention.

[0025] In an example implementation, MCG's CPX8216IP or CPX1204IP chassis, which are compact PCI chassis, are used. The CPX8216IP is a 16 slot 12RU chassis while the CPX1204IP is a five slot 3RU chassis.

[0026] A number of input/output (I/O) slots 102-124 are provided, along with CPU slots 126, 128 and bridge slots 130, 132.

[0027] Moreover, these chassis have two communication buses in the backplane:

(1) Compact PCI (cPCI), 64 bits wide at 33 MHz;
(2) IP interconnect; a serial path for data to be sent from any board to any board at 125 MHz.

[0028] FIG. 2 illustrates a broadband audio/video/data router in accordance with the present invention.

[0029] A remote input multiplex (e.g., ten channels) is provided to an input processor card 204. The multiplex may be provided via a remote transmission, or from a local storage device, for example. Note that additional input cards may be provided to handle additional input multiplexes. The input card 204 includes a function 206 that provides data-to-IP conversion and PID filtering (e.g., dropping of specific packets in a channel based on their PID). Data-to-IP conversion refers to encapsulating packets into an IP-like format, as described below particularly in connection with FIG. 4. A router 208 may be a 24-port router that is configured to output the ten input channels on any of fourteen output paths to an IP segment 202 of the backplane 100. Of course, the configuration discussed is an example only, as many variations will be apparent to those skilled in the art. The IP backplane segment 202 communicates with any number of other cards in the chassis, such as example cards 210 and 220 for performing some desired target processing of the recovered packets.

[0030] The card 210, which is configured as a mux card in the present example, includes a function 213 that provides IP-to-data conversion, PID aliasing, and a PCI-to-PCI bridge 216. IP-to-data conversion refers to decapsulating the encapsulated packets received from the input card 204. An output 215 of the card 210 is provided.

[0031] Similarly, the card 220, which is configured as a transcoder card in the present example, includes a function 223 that provides IP-to-data conversion, PID

aliasing, and a PCI-to-PCI bridge 226.

[0032] The card 210 may also include two example DSPs 214 for performing multiplexing, while the card 220 includes four example DSPs 224, each for performing transcoding. However, the cards 210, 220 may include processing circuitry for performing any desired processing/modification of the packets.

[0033] Moreover, the cards 210, 220 includes respective routers 212, 222 that receive the packets from the router 208 of the input card 204. The routers 212, 222 route the received packets to the functions 213, 223, respectively, for subsequent use at the respective DSPs using techniques that are discussed further below.

[0034] It is also possible to provide additional cards similar to the cards 210, 220 in the chassis. For example, if additional transcoding resources are need, additional cards such as the card 220 may be provided.

[0035] The routers 208, 212, and 222 may comprise off-the-shelf IP routers that are modified in accordance with the present invention.

[0036] A processor board 250 comprises a host computer for the entire system. For example, Motorola's 366 MHz MPC750 may be used.

[0037] The CPX8216IP and CPX1204IP model chassis have two independent communication pathways: [1] the cPCI 240 bus allowing for configuration and control, and the passage of compressed bitstreams to the mux, and [2] the IP interconnect 202 allowing for incoming data to be distributed to any card. Based on the need to route MPEG2 packets to any processor (DSP) on any board, the IP interconnect 202 is taken advantage of so as to serve as an MPEG2 router. This is made possible by installing routers (such as 212, 222) on the cards. By having a router on every board, maximum flexibility is achieved for routing any packet anywhere. Any incoming packet can be routed to any target processor device on any target card. Moreover, both chassis models may have a Motorola 750 PowerPC-based CPU card 250.

[0038] Generally, the invention provides a way to move packets between cards based on the desired manipulation/processing that is carried out at the cards. The packets are routed using a customized IP-like protocol.

[0039] FIG. 3 illustrates the input processor card of FIG. 2 in accordance with the present invention.

[0040] As mentioned, the Input Card's (INP) 204 primary function is to accept up to, e.g., 10 MPEG2 data streams, perform PID filtering and encapsulate the recovered packets over a customized IP packet using the encapsulation/routing protocol of the present invention.

[0041] FIG. 3 shows specific components and signals in an example embodiment. The router chipset 208 is a 24-port router that is configured as 10x14 (10 inputs, 14 outputs). An FPGA 310 provides a loadable IP Ethernet template via PCI, and builds a customized Ethernet/IP packet around MPEG2 data for SMII interface to the router at 125MHz. The FPGA 310 may handle ten SMII interfaces to the router at 125 MHz.

[0042] FIG. 4(a) illustrates an encapsulated MPEG transport packet in accordance with the present invention. An Ethernet IP-like template 400 (encapsulating packet) surrounds the MPEG2 transport packet 450, with PID field 452 (encapsulated packet).

[0043] The destination IP address 410 is used to carry the exact packet source, which is comprised of [1] board slot, [2] spigot/port number, and [3] the 13-bit original MPEG2 packet PID (oPID) with leading three bits of zeros. This field identifies the source of the packet throughout the routing chain. The notation "oPID:oPID" refers to two eight-bit fields that carry the 13-bit PID. The destination IP address is unique for each and every component within a transport stream. A memory lookup based on this field is performed to determine which one of 14 outputs the packet is to be routed to. The destination IP address field is again used later in the TRC and MUX board for PID aliasing. The routing table of the router is programmed by way of PCI by the host CPU. Any packet can be routed back to the host via the PCI backbone.

[0044] FIG. 4(b) illustrates a method for routing a packet, and providing PID aliasing, in accordance with the present invention. At box 470, an incoming MPEG packet is received at the input card (e.g., card 204 in FIG. 2). At box 472, and IP header is built that provides information regarding the source of the MPEG packet in an IP destination address field. At box 474, an input processor at the input card handles the encapsulated MPEG packet, and provides it to a router. In particular, at box 476, a lookup is performed to determine which target board(s) the packet is to be routed to. Such a lookup may be configured by the host CPU to efficiently allocate the packets among the available resources of the target processing boards.

[0045] When the packet is received at the target board (s), it is processed at a router there (box 478). At box 480, another lookup is performed to obtain a PID alias value as a function of the destination IP address, again, where the lookup is configured by the host CPU, e.g., via the PCI at the time of system power-up. The PID alias value is provided in a destination MAC address field of the modified encapsulating IP packet.

[0046] An additional return value of this lookup is a specified target port for hardware on the card. At box 482, the processing card router provides the encapsulating packet to the specified target port of packet hardware on the card. For example, in the specific example of FIG. 2, the transcoder card 220 has four ports and the mux card 210 has two ports.

[0047] At box 484, the packet hardware decapsulates the customized IP packet, and substitutes the PID alias value for the original PID in the encapsulated MPEG packet (in the field 452).

[0048] At box 486, the IP header is stripped leaving the packet hardware, thereby yielding the MPEG packet in its native form. At box 488, the MPEG packet is sent to the DSP associated with the specified target port for

further processing. The processed MPEG packet may ultimately be provided in an output transport stream for receipt by a decoder.

[0049] FIG. 5 illustrates a processing card for transcoding, muxing or other processing, in accordance with the present invention.

[0050] The example shows the transcoding card 220 of FIG. 2, where four DSPs 224 are provided.

[0051] Accordingly, it can be seen that the present invention provides an efficient, integrated solution for processing input transport streams, such as MPEG2 streams. The invention provides PID aliasing in a system where MPEG packets are routed among various cards in a chassis to provide target processing functions such as transcoding, multiplexing, splicing, scrambling, and so forth. Customized IP-type routing is used to route the packets among the cards. A packet with any PID can be routed to any target MPEG2 processing engine on any board across a backplane. The system may use off-the-shelf components to improve cost effectiveness and reduce development time.

[0052] Furthermore, PID aliasing is performed by taking advantage of the architecture of an IP router on a target processor card to embed values within an IP packet based on the destination IP address. A memory lookup based on the destination IP address is used to indicate which one of multiple outputs and, in turn, target processors the packet is to be routed to. The aliased PID is embedded in the destination MAC address as the packet is sent out of the IP router. These parameters are programmed by a host CPU via PCI.

[0053] Moreover, by having PID aliasing embedded within the IP router, ten 32Kbyte DPRAMs on the input processing card are eliminated, compared to some conventional systems, which in turn lowers cost and increases reliability since there are fewer components that can fail.

[0054] Although the invention has been described in connection with various preferred embodiments, it should be appreciated that various modifications and adaptations may be made thereto without departing from the scope of the invention as set forth in the claims.

[0055] For example, while specific hardware has been identified herein for implementing the present invention, any suitable substitute hardware/software that provides an analogous functionality may be used.

Claims

1. A processing circuit card apparatus receivable in a chassis, and adapted to receive data from an input card in the chassis via a backplane, comprising:

means for receiving at least one encapsulating packet from the input card, wherein the encapsulating packet encapsulates a packet of digital data recovered from a transport stream, and comprises a first field that contains source information regarding the recovered packet;

wherein the encapsulated packet includes an original packet identifier therein;

means for providing a packet identifier alias value in accordance with the source information in the first field;

means for inserting the packet identifier alias value into a second field of the encapsulating packet;

means for retrieving the packet identifier alias value from the second field, and replacing the original packet identifier in the encapsulated packet with the packet identifier alias value; and

means for decapsulating the encapsulated packet with the packet identifier alias value therein to provide a corresponding decapsulated packet.

2. The apparatus of claim 1, wherein:

said first field comprises a destination address field.

3. The apparatus of claim 1 or 2, wherein:

the encapsulating packet is provided according to a customized Internet Protocol.

4. The apparatus of one of claims 1 to 3, wherein:

the transport stream is provided according to a broadband communication scheme.

5. The apparatus of one of claims 1 to 4, wherein:

the chassis is provided at a headend of a broadband communication network.

6. The apparatus of one of claims 1 to 5, wherein:

the source information comprises a source slot from which the packet of digital data is recovered.

7. The apparatus of one of claims 1 to 5, wherein:

the source information comprises a source port from which the packet of digital data is recovered.

8. The apparatus of one of claims 1 to 5, wherein:

the source information comprises the original packet identifier.

9. The apparatus of one of claims 1 to 8, wherein:

the means for providing the packet identifier alias value performs a lookup to obtain the packet identifier alias value based on the source information.

10. The apparatus of claim 9, wherein:

the lookup is configured by a system host computer.

11. The apparatus of one of claims 1 to 10, wherein:

the second field comprises a destination medium access control (MAC) address.

12. The apparatus of one of claims 1 to 11, wherein the retrieving and replacing means, and the decapsulating means are each provided in a plurality of different processing paths, further comprising:

a router for routing the encapsulating packet with the packet identifier alias value therein to a selected one of the processing paths for processing thereat.

13. The apparatus of claim 12, wherein:

the router selects the selected processing path in accordance with the source information in the first field.

14. The apparatus of claim 13, wherein:

the router is configured by a system host computer for performing the selection.

15. The apparatus of one of claims 12 to 14, wherein:

the router has a plurality of output ports, each output port coupled to one of the processing paths.

16. The apparatus of one of claims 12 to 15, wherein:

each of the processing paths comprises a target processing function.

17. The apparatus of claim 16, wherein:

the target processing functions are common in the different processing paths.

18. The apparatus of one of claims 12 to 17, wherein:

the router comprises a lookup table for selecting the processing path on which to route the encapsulating packet.

19. A method for processing data at a processing circuit card that is receivable in a chassis, and adapted to receive data from an input card in the chassis via a backplane, comprising the steps of:

receiving at least one encapsulating packet from the input card, wherein the encapsulating packet encapsulates a packet of digital data recovered from a transport stream, and comprises a first field that contains source information regarding the recovered packet;

wherein the encapsulated packet includes an original packet identifier therein;

providing a packet identifier alias value in accordance with the source information in the first field;

inserting the packet identifier alias value into a second field of the encapsulating packet;

retrieving the packet identifier alias value from the second field, and replacing the original packet identifier in the encapsulated packet with the packet identifier alias value; and

decapsulating the encapsulated packet with the packet identifier alias value therein to provide a corresponding decapsulated packet.

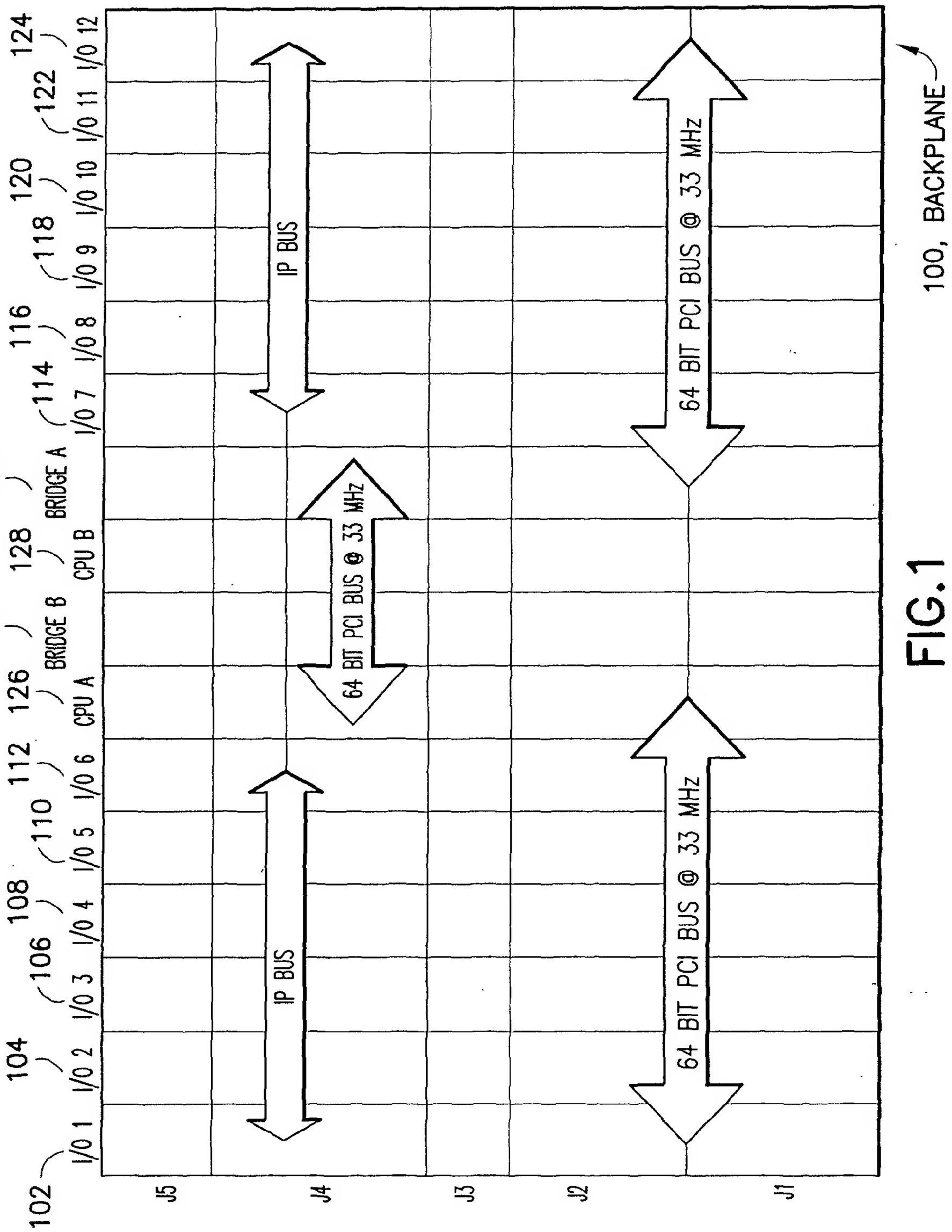
100, BACKPLANE
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
132
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
I/O 6
I/O 7
I/O 8
I/O 9
I/O 10
I/O 11
I/O 12
CPU A
BRIDGE B
CPU B
BRIDGE A
IP BUS
IP BUS
64 BIT PCI BUS @ 33 MHz
64 BIT PCI BUS @ 33 MHz
64 BIT PCI BUS @ 33 MHz
64 BIT PCI BUS @ 33 MHz
J5
J4
J3
J2
J1

FIG.1

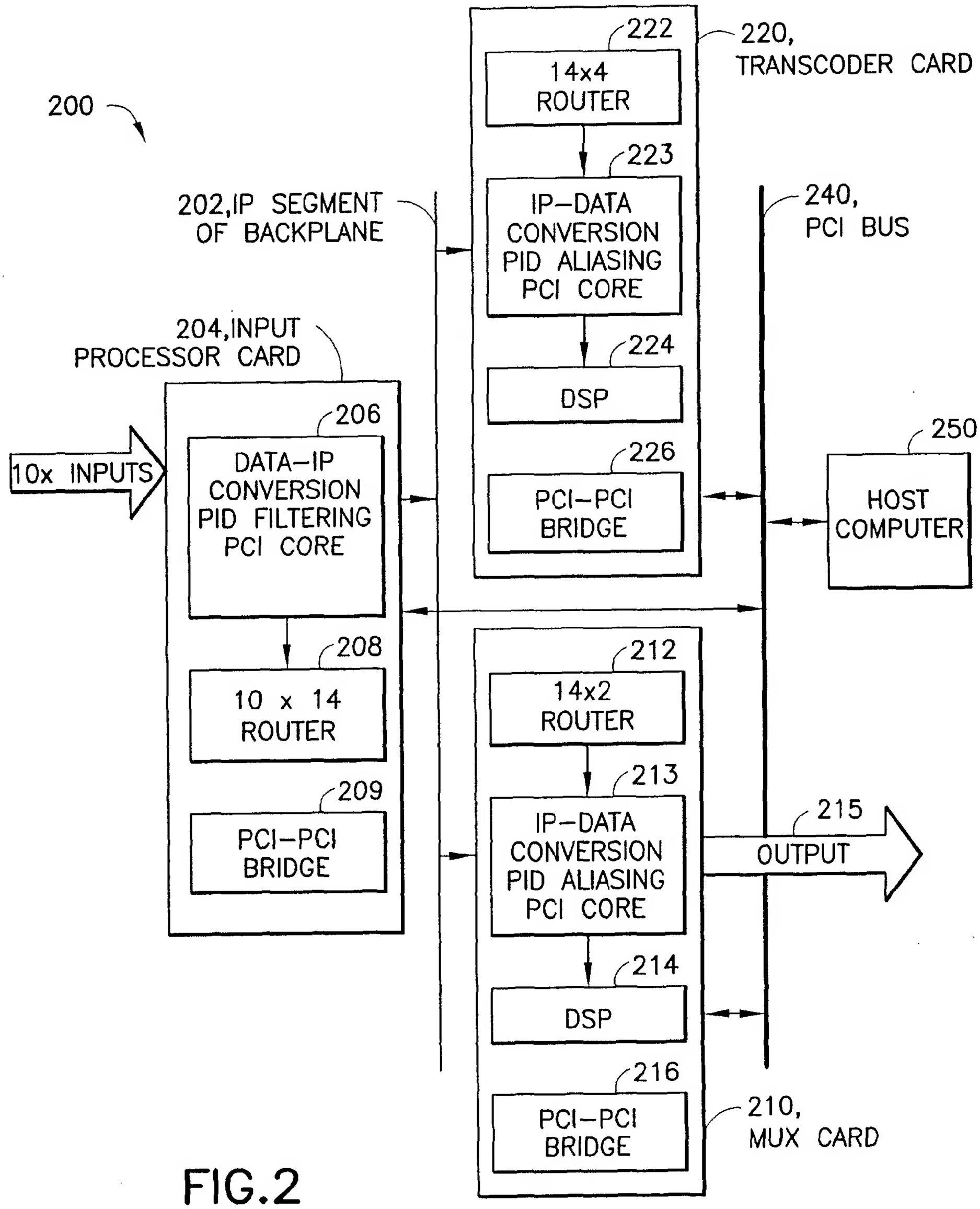
200
202,IP SEGMENT OF BACKPLANE
204,INPUT PROCESSOR CARD
10x INPUTS
206
DATA–IP CONVERSION PID FILTERING PCI CORE
208
10 x 14 ROUTER
209
PCI–PCI BRIDGE
222
14x4 ROUTER
220, TRANSCODER CARD
223
IP–DATA CONVERSION PID ALIASING PCI CORE
224
DSP
226
PCI–PCI BRIDGE
240, PCI BUS
250
HOST COMPUTER
212
14x2 ROUTER
213
IP–DATA CONVERSION PID ALIASING PCI CORE
215
OUTPUT
214
DSP
216
PCI–PCI BRIDGE
210, MUX CARD

FIG.2

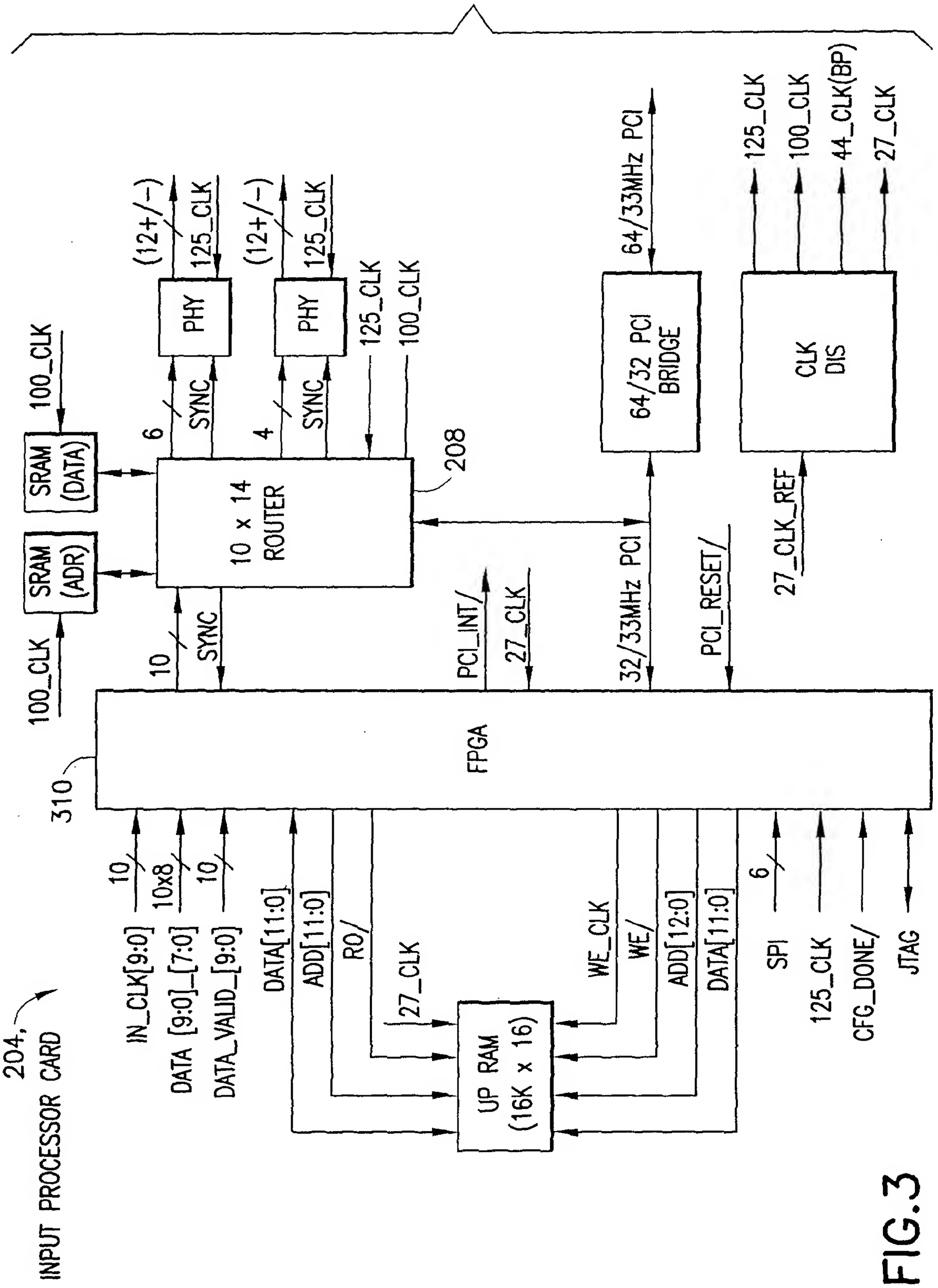
204,
INPUT PROCESSOR CARD
IN_CLK[9:0]
DATA [9:0]_[7:0]
DATA_VALID_[9:0]
DATA[11:0]
ADD[11:0]
RO/
27_CLK
UP RAM
(16K x 16)
WE_CLK
WE/
ADD[12:0]
DATA[11:0]
SPI
125_CLK
CFG_DONE/
JTAG
310
FPGA
100_CLK
SRAM (ADR)
SRAM (DATA)
10 x 14 ROUTER
208
10
10x8
6
4
SYNC
(12+/-)
125_CLK
PHY
PCI_INT/
27_CLK
32/33MHz PCI
PCI_RESET/
64/33MHz PCI
64/32 PCI BRIDGE
100_CLK
125_CLK
44_CLK(BP)
27_CLK
CLK DIS
27_CLK_REF

FIG.3

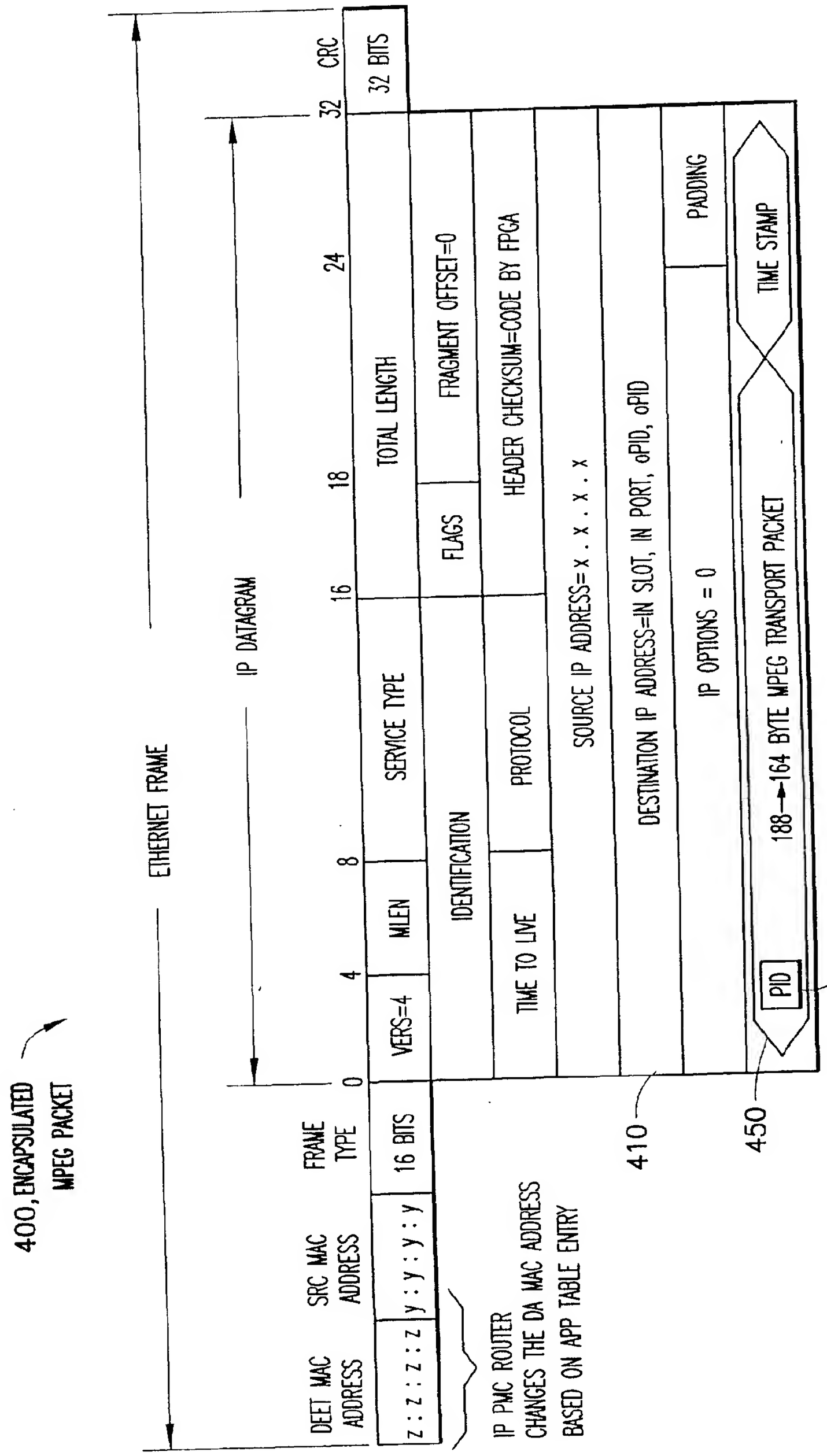
400, ENCAPSULATED MPEG PACKET
ETHERNET FRAME
IP DATAGRAM
0
4
8
16
18
24
32
VERS=4
MLEN
SERVICE TYPE
TOTAL LENGTH
IDENTIFICATION
FLAGS
FRAGMENT OFFSET=0
TIME TO LIVE
PROTOCOL
HEADER CHECKSUM=CODE BY FPGA
SOURCE IP ADDRESS= x . x . x . x
DESTINATION IP ADDRESS=IN SLOT, IN PORT, oPID, oPID
IP OPTIONS = 0
PADDING
TIME STAMP
PID
188→164 BYTE MPEG TRANSPORT PACKET
452
410
450
DEET MAC ADDRESS
SRC MAC ADDRESS
FRAME TYPE
z : z : z : z : z
y : y : y : y
16 BITS
IP PMC ROUTER
CHANGES THE DA MAC ADDRESS
BASED ON APP TABLE ENTRY

FIG.4a

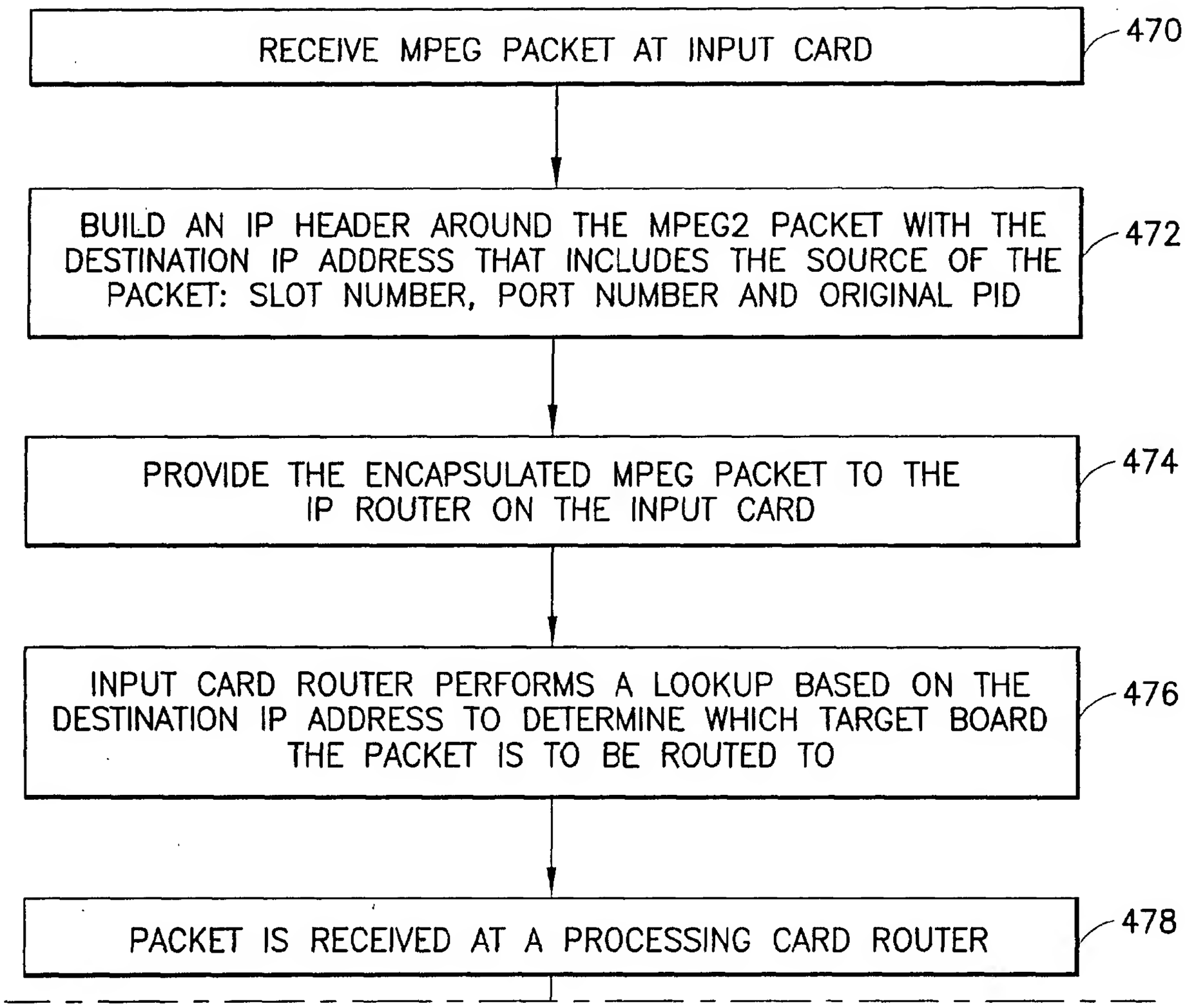

FIG.4b-1

FIG.4b-1

FIG.4b

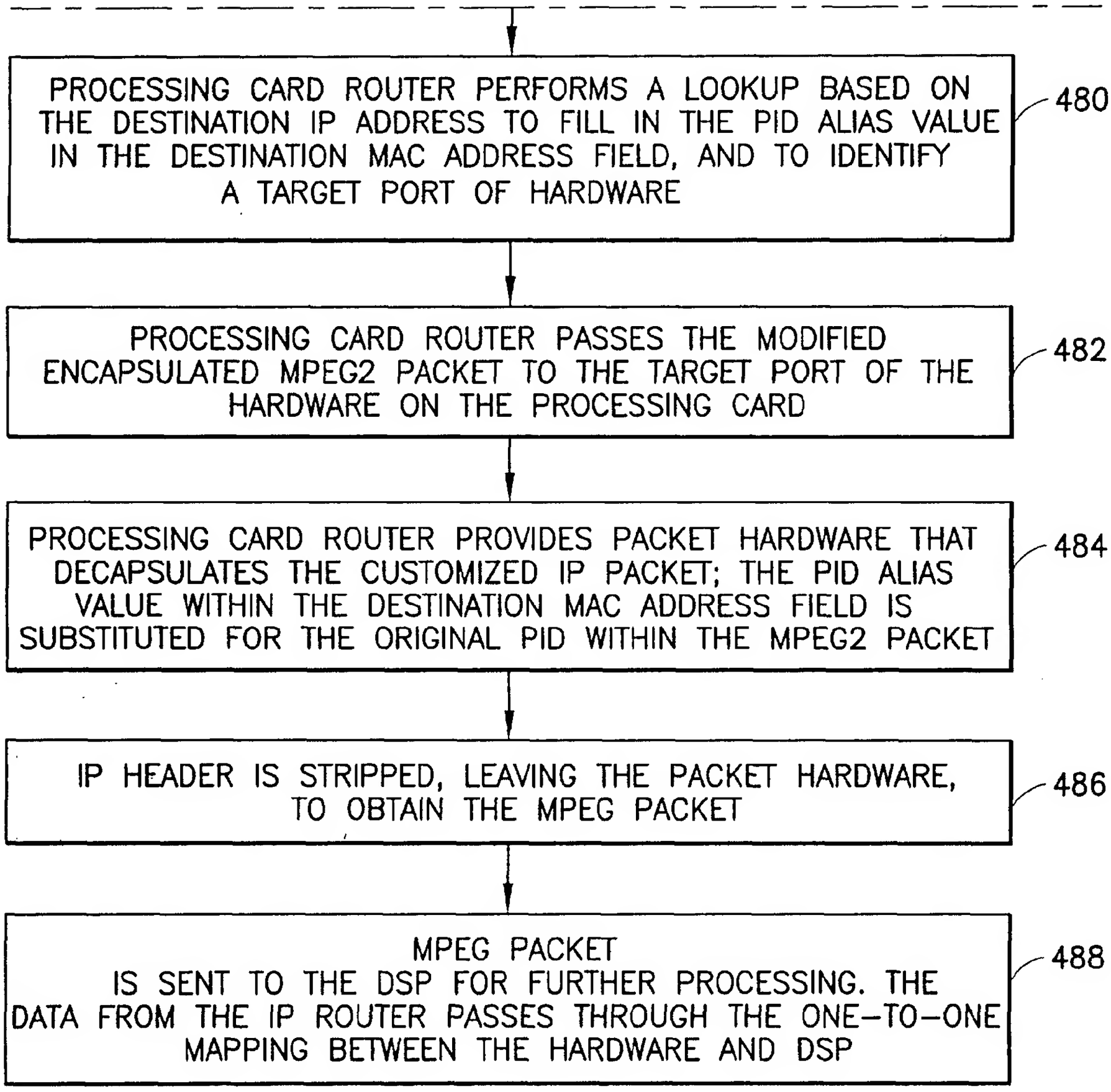
PROCESSING CARD ROUTER PERFORMS A LOOKUP BASED ON THE DESTINATION IP ADDRESS TO FILL IN THE PID ALIAS VALUE IN THE DESTINATION MAC ADDRESS FIELD, AND TO IDENTIFY A TARGET PORT OF HARDWARE
480
PROCESSING CARD ROUTER PASSES THE MODIFIED ENCAPSULATED MPEG2 PACKET TO THE TARGET PORT OF THE HARDWARE ON THE PROCESSING CARD
482
PROCESSING CARD ROUTER PROVIDES PACKET HARDWARE THAT DECAPSULATES THE CUSTOMIZED IP PACKET; THE PID ALIAS VALUE WITHIN THE DESTINATION MAC ADDRESS FIELD IS SUBSTITUTED FOR THE ORIGINAL PID WITHIN THE MPEG2 PACKET
484
IP HEADER IS STRIPPED, LEAVING THE PACKET HARDWARE, TO OBTAIN THE MPEG PACKET
486
MPEG PACKET IS SENT TO THE DSP FOR FURTHER PROCESSING. THE DATA FROM THE IP ROUTER PASSES THROUGH THE ONE–TO–ONE MAPPING BETWEEN THE HARDWARE AND DSP
488

FIG.4b–2

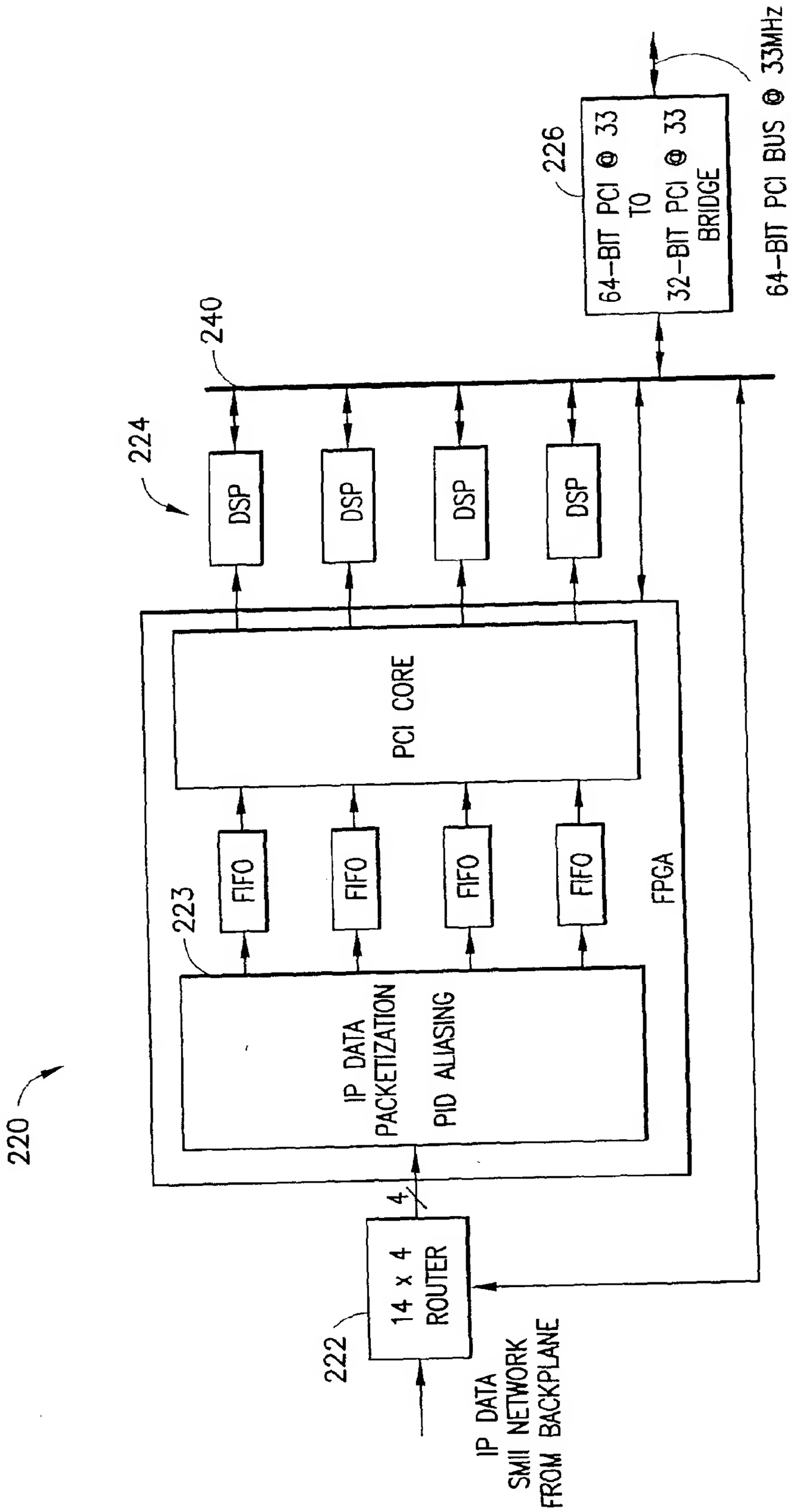
220
240
224
DSP
DSP
DSP
DSP
226
64-BIT PCI @ 33
TO
32-BIT PCI @ 33
BRIDGE
64-BIT PCI BUS @ 33MHz
TO BACKPLANE
223
FIFO
FIFO
FIFO
FIFO
PCI CORE
IP DATA
PACKETIZATION
PID ALIASING
FPGA
4
222
14 x 4
ROUTER
IP DATA
SMII NETWORK
FROM BACKPLANE

FIG.5

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EUROPEAN SEARCH REPORT

Application Number
EP 01 12 4854

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	15 April 2002	Fantini, F

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